

The Method of Bandwidth Extension of SiGe BiCMOS Microwave Variable-Gain Amplifier Integrated Circuit

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The article proposes a method of bandwidth extension of the analog integrated circuit of the variable-gain amplifier (VGA) based on SiGe BiCMOS technology with the rules of 0.18 μm . The designed VGA has a linear (in dB) control characteristic. The authors consider the VGA architecture and present its design outputs. They describe the properties of two modifications of the VGA integrated circuit — with classical correction of the response and with the circuit of the parasitic capacitance cancellation in the high-impedance node. The article shows that the second circuit solution allows increasing the upper frequency limit of the VGA by a factor of 1.8-2.

Key words: variable-gain amplifier; “folded” cascode; operational amplifier; SiGe BiCMOS technology; R-2R matrix; cancellation; upper frequency limit

Introduction

Variable gain amplifiers (VGAs) play an important role in modern transceivers of communication systems and medical equipment. They are applied in design of various circuits with automatic gain control [1–3].

To extend bandwidth of analog integrated circuits and their functional nodes in modern microelectronics, the method of parasitic capacitance compensation [4–10] is used, which is developed in the articles [11–16].

In connection with wide application of SiGe transistors, as well as their satisfactory operation at low temperatures [17–19] and exposure to radiation [20,21], i.e. in sensor interfaces [9], it is of interest to investigate the possibilities of compensation circuits in analog SiGe circuits of microwave range.

The aim of the article is to discuss frequency correction features as well as comparative computer simulation results of SiGe microwave variable gain amplifier, in which the principle of parasitic capacitance cancellation is used in the high impedance node of one of the functional nodes — the “current/voltage” converter based on the “folded” cascode to increase the upper frequency limit.

1 The Schematic Structure of SiGe BiCMOS Variable Gain Amplifier

The designed VGA circuit (Fig. 1a) contains a broadband passive attenuator (from 0 dB to –48.16 dB) with input differential stages (R-2R network, Fig. 1b) a fixed-gain amplifier (OA circuit), a gain control interface (scaler), a reference current source (src) and also resistors of feedback R1-R7.

The scheme of VGA (Fig. 1a) has the following pins: VINP - VGA input; *sd* — reference current source (RCS) on/off (when *sd* is connected to gnd, RCS turns on, when *sd* and *Vcc* are shorted, it turns off); GPOS, GNEG - gain factor control pins; VOUT - VGA output; FDBK - feedback pin; VCC, gnd - supply voltage and global bus pins. Half of the supply voltage is fed to the GNEG and *Vbias* pins.

VGA operates in two modes:

- High - an increased gain mode (FDBK pin isn't connected);
- Low - a normal mode (FDBK pin is shorted to VOUT pin).

The gain control interface (“scaler” IP-module, Fig. 1a) is a voltage/current converter, the slope of which depends on the resistance of local negative feedback resistor.

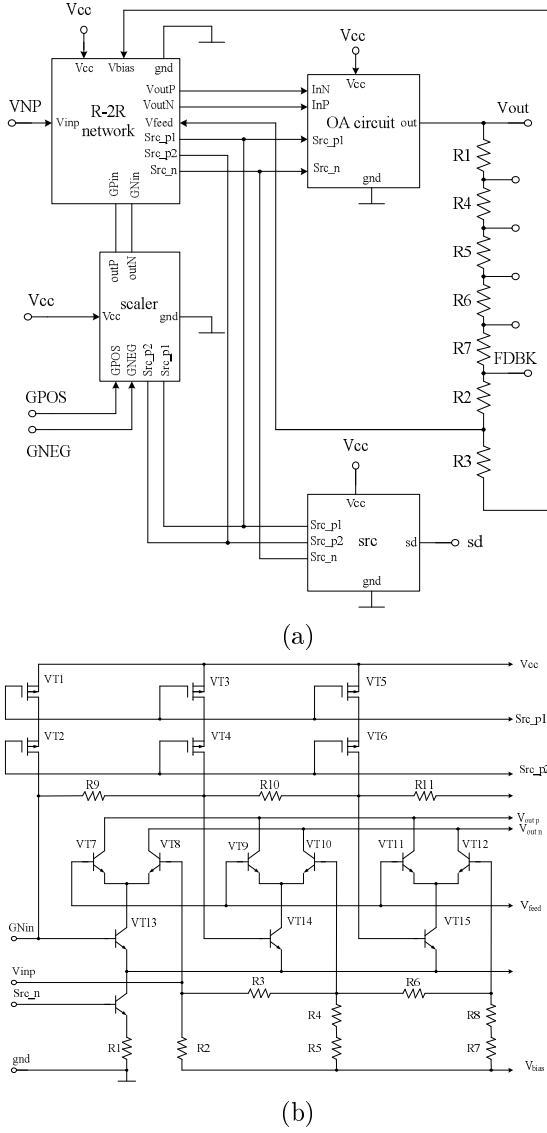


Fig. 1. The schematic structure of VGA (a) and the general view of R-2R matrix with differential stages (b)

“OA circuit” IP-module provides the output current signal conversion of differential stages (Fig. 1b) into voltage.

2 The Method of Parasitic Capacitance Compensation in the High Impedance Node of Operational Amplifier

In the designed VGA, the principle of C_{01} cancellation of parasitic capacitance in the high impedance node Σ_1 (Fig. 2a) is used. The idea of the bandwidth extension involves connection of some compensation circuit with the transfer function $S_c(p)$ (Fig. 2b) to the high impedance node Σ_1 [11–16]. This circuit provides compensation of the C_{01} effect on the low-signal characteristics of the amplifier — the upper

frequency limit f_{cutoff}^* (at the level of -3 dB) and the desired transient time t_{stab}^* .

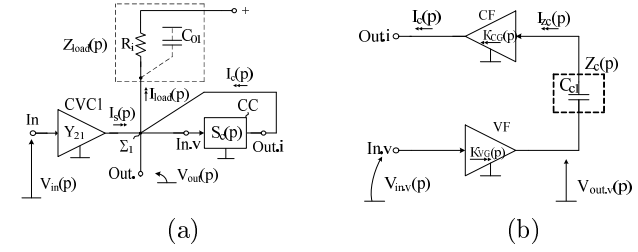


Fig. 2. The flowchart of the standard amplifier output circuit (a) and the example of the compensation circuit design (b).

At the desired transient time, which must be small ($t_{stab}^* \rightarrow 0$), at the given values of C_{01} and the upper frequency limit of the corrected amplifier f_{cutoff}^* as well as at the known frequency f_{cutoff} of the uncorrected amplifier, C_{c1} capacitance of compensation circuit should be chosen from the following equations:

$$C_{c1} = C_{01} \left[\frac{1}{K_{VG}K_{CG}} - \frac{t_{stab}^*}{t_{stab}} \right], \quad (1)$$

$$C_{c1} = \frac{C_{01}}{K_{VG}K_{CG}} (1 - f_{cutoff}/f_{cutoff}^*)$$

where $K_{VG} < 1$, $K_{CG} < 1$ — transfer ratios of the voltage followers (VF) and the current followers (CF); $t_{stab} = 2\pi R_1 C_{01}$ — transient time without compensation circuit.

Besides, taking into account the compensation circuit effect, the upper frequency limit f_{cutoff}^* of the amplifier (Fig. 2a) is determined by the following formula:

$$f_{cutoff}^* = \frac{1}{2\pi R_i [C_{01} - K_{CG}K_{VG}C_{c1}]}. \quad (2)$$

Fig. 3 shows the scheme of “OA-circuit” module with the parasitic capacitance C_{01} compensation in the high-resistance node of the current mirror at transistors Q3-Q6.

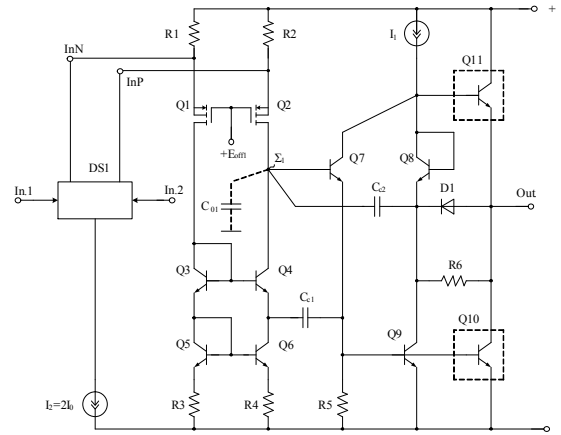


Fig. 3. The “OA_circuit” “voltage/current” converter scheme with parasitic capacitance compensation circuit.

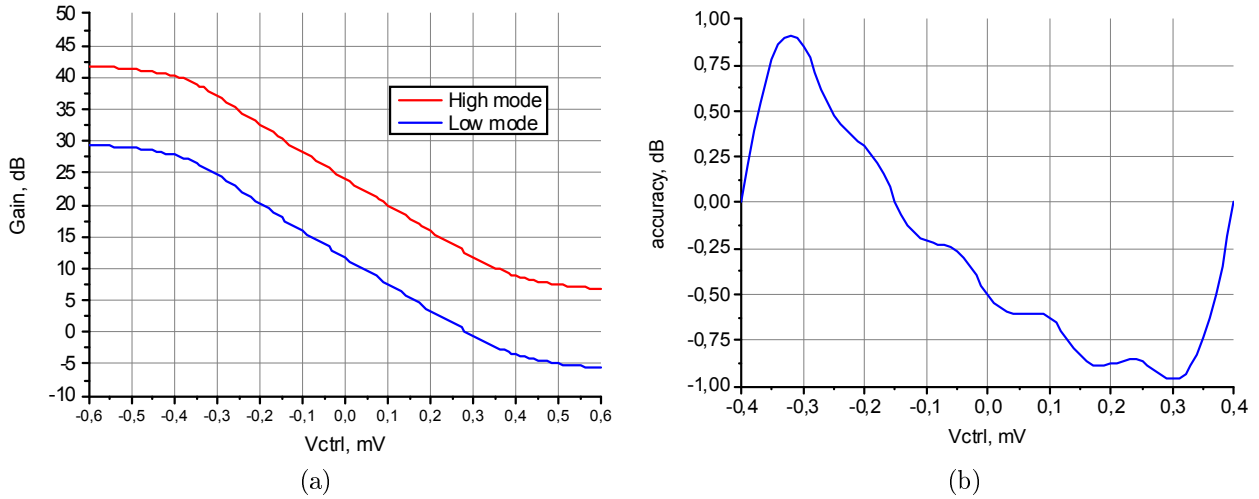


Рис. 4. The range of regulation of VGA in HIGH and LOW modes, when $f_x = 140$ MHz, (a) and the dependence of regulation accuracy on the control voltage (V_{ctrl}) (b)

According to Fig. 3 the compensation circuit includes the voltage follower based on transistor Q7, the current follower based on transistor Q4 and the capacitance $C_{c1} = 400 fF$. To increase the stability of the amplifier the conventional correction capacitance $C_{c2} = 200 fF$ is provided.

3 The Computer Simulation

The comparative computer simulation results of two versions of the frequency correction of VGA in Cadence Virtuoso environment on SiGe Bi-CMOS models (250 nm) of transistors are given in Fig. 5.

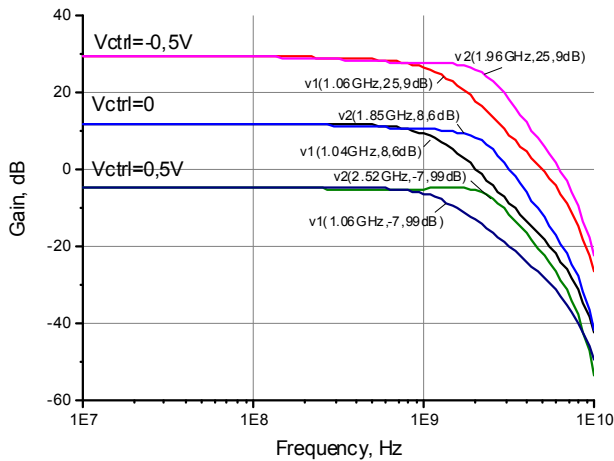


Рис. 5. The dependence of the gain factor on the control voltage in VGA with classical correction (v1) and cancellation (v2).

They show the increase of the upper frequency limit by a factor of 1.8 – 2.

The regulating characteristics of VGA in the mode of low and high gain are presented in Fig. 4a.

The regulation errors are described in the diagram of Fig. 4b.

The accuracy of the gain control ΔK_V is estimated by the formula $\Delta K_V = \max(\Delta K_{V_i})$, which can be presented as

$$\Delta K_V = \frac{20 \log K_{V_i}}{K_{V_{max}}} + \frac{20 \log K_{V_{max}}}{K_{V_{min}}} \left[\frac{V_{cmax} - V_{ci}}{V_{cmax} - V_{cmin}} \right] \quad (3)$$

where K_{V_i} — gain factor at the i -th value of the control voltage V_{ci} ($i = 1 \dots 20$).

Fig. 6 shows that the proposed correction circuit allows increasing its bandwidth by a factor of 1.8 – 2 in the whole range of control voltages up to $f_B^* = 1.85 \div 2.5$ GHz.

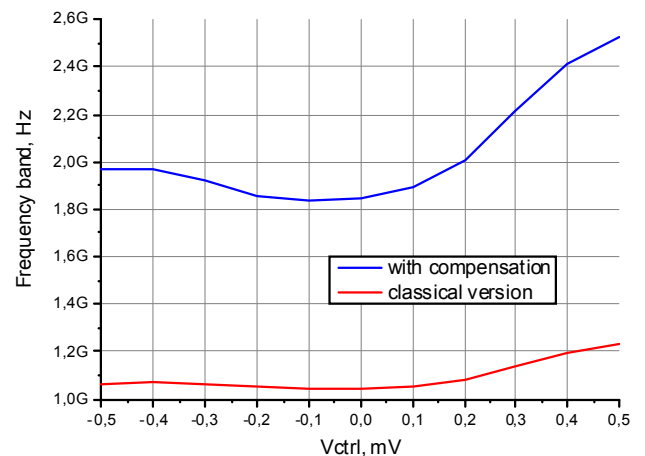


Рис. 6. The dependence of the upper frequency limit of VGA on the control voltage (V_{ctrl}) with the proposed (version 2) and classical (version 1) correction.

Fig. 7 shows the dependences of output power of VGA on the input power and also the output 1 dB compression point.

Табл. 1 The combined parameters of VGA with two versions of correction circuits

	Regulation range, dB/V	Upper frequency limit, GHz	Regulation accuracy, dB		1 dB compression point, dBm	OIP3, dBm	Current consumption, mA	Supply voltage, V
Conditions	$V_{ctrl} = \pm 450$ mV, $f_x = 140$ MHz	$V_{ctrl} = 0$	$V_{ctrl} = \pm 400$ mV	$V_{ctrl} = \pm 450$ mV	$f_x = 140$ MHz, $V_{ctrl} = -0.5$ V	$f_x = 140$ MHz, $V_{ctrl} = -0.5$ V	$V_{cc} = 5$ V	
VGA with classical correction	36.6	1.04	± 0.95	± 1.7	12	26	22	4.5-5.5
VGA with compensation	36.6	1.85	± 0.95	± 1.7	12	26	22	4.5-5.5

$R_{load} = 100$ Ohm, $C_{load} = 3$ pF, $T = 27$ °C.

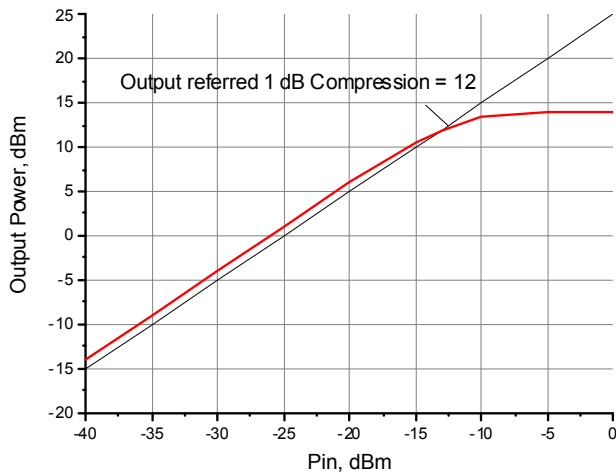


Рис. 7. The dependence of the output power on the input power for VGA of the second version, when $V_{ctrl} = -0.5$ V.

Fig. 8 shows that VGA can operate at supply voltage range of 4.5 – 5.5 V and temperature range from –60 to 150 degrees (basic temperature range).

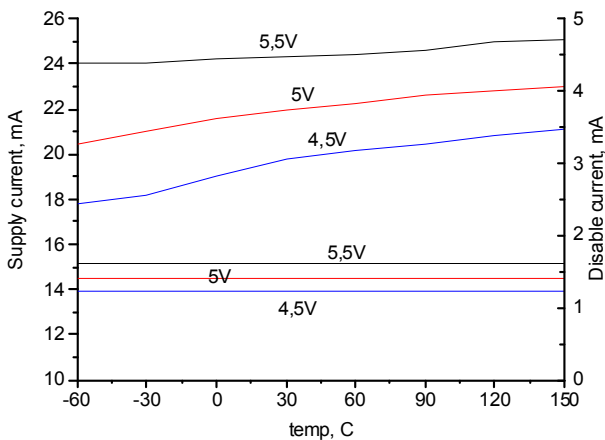


Рис. 8. The current consumption at various $V_{cc} = 4.5 - 5.5$ V.

Summary

The article shows the prospects of application of parasitic capacitance compensation circuits in high impedance nodes in SiGe analog integrated circuits.

The SiGe BiCMOS variable gain amplifier integrated circuit with linear (in dB) characteristic is designed according to the rules of 0.18 μ m, which has the following main parameters:

- regulation accuracy $\pm 0.95 \div 1.7$ dB;
- upper frequency limit 1.85 GHz;
- tuning range 36.6 dB;
- 1 dB compression point 12 dBm;
- control voltage ± 450 mV.

The proposed method of parasitic capacitance compensation in VGA increases its upper frequency limit by 1.8 – 2 times.

Taking into account high radiation hardness of SiGe transistors [20, 21] as well as their satisfactory characteristics at low temperatures [17–19], the designed VGA should be recommended for the extended application in communication devices and automatics, including those ones, which operate in the demanding environment.

Acknowledgments

The research was carried out at the expense of the Grant of the Russian Science Foundation (project No. 16-19-00122).

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Метод розширення діапазону робочих частот SiGe БіКМОН НВЧ мікросхеми регульованого підсилювача

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Запропоновано метод розширення діапазону робочих частот аналогової мікросхеми регульованого підсилювача (РП) за SiGe БіКМОН технології з проектними нормами 0,18 мкм. Розроблений РП має лінійну (в дБ) характеристику управління. Розглядається архітектура РП і наводяться результати його проектування. Описано властивості двох модифікацій мікросхеми РП — з класичною корекцією амплітудно-частотної характеристики і з ланцюгом взаємної компенсації паразитної ємності у високоімпедансному вузлі. Показано, що друге схематичне рішення дозволяє збільшити верхню граничну частоту РП в 1,8-2 рази.

Ключові слова: регульований підсилювач; “перегнутий” каскод; операційний підсилювач; SiGe БіКМОН технологія; матриця R-2R; взаємна компенсація; верхня гранична частота

Метод расширения диапазона рабочих частот микросхемы SiGe БиКМОП СВЧ регулируемого усилитель

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Прокopenко Н. Н.*

Предлагается метод расширения диапазона рабочих частот аналоговой микросхемы регулируемого усилителя (РУ) по SiGe БиКМОП технологии с проектными нормами 0,18 мкм. Разработанный РУ имеет линейную (в дБ) характеристику управления. Рассматривается

архитектура РУ и приводятся результаты его проектирования. Описаны свойства двух модификаций микросхемы РУ — с классической коррекцией амплитудно-частотной характеристики и с цепью взаимной компенсации паразитной емкости в высокоимпедансном узле. Показано, что второе схемотехническое решение позволяет увеличить верхнюю граничную частоту РУ в 1,8-2 раза.

Ключевые слова: регулируемый усилитель; “перегнутый” каскод; операционный усилитель; SiGe БиКМОП технология; матрица R-2R; взаимная компенсация; верхняя граничная частота