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The Experimental Study of the Cerium Dioxide - Silicon Interface of MIS Structures

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The article is devoted to the actual task of studying a dielectric, which is an alternative to silicon dioxide in metal-insulator-semiconductor (MIS) structures. In metal-silicon dioxide-silicon structures, upon going to nanosize, the thickness of the dielectric film decreases so much that it becomes tunnel-transparent and its breakdown voltage decreases. These phenomena can be eliminated by replacing silicon dioxide with a dielectric with a higher dielectric constant. These dielectrics primarily include oxides of transition and rare-earth metals. The parameters and characteristics of the MIS structure are determined by various factors, but the properties of the dielectric and the dielectric-semiconductor interface play a special role. In previous works of the authors, it was theoretically proved that cerium dioxide from a number of candidate dielectrics should have the best quality of the interface with silicon. This work is devoted to a study aimed at determining the flat-band voltage and capacitance of MIS structures and at assessing the quality of the cerium dioxide-silicon interface. The study is carried out by the method of capacitance-voltage characteristics. For this, the high-frequency capacitance-voltage characteristics of the aluminum – cerium dioxide – silicon structures were measured at different temperatures. The capacity of the space charge region (SCR) in the enrichment and weak inversion modes of the near-surface layer of a semiconductoris considered. It is shown that the dependence of this capacitance in the (–2) degree on the voltage at the metal electrode $c_s^{-2}(V_G)$ is linear. The intersection of this line with the abscissa axis makes it possible to determine the flat-band voltage. The slope tangent of this linear dependence makes it possible to determine the energy density of the charge at the dielectric–semiconductor interface. It is shown that the charge density at the cerium dioxide – silicon interface corresponds to the minimum values of the charge density at the silicon dioxide – silicon interface. The absence of a shift in the capacitance-voltage characteristics of the structures under study with a change in temperature indicates the stability of the charge at the cerium dioxide - silicon interface.

Key words: MIS structure; cerium dioxide; capacitance-voltage characteristic (CV characteristic); flat-band voltage; charge density at the dielectric-semiconductor interface

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Introduction

The basis of modern micro- and nanoelectronics is metal-insulator-semiconductor (MIS) structures. The parameters and characteristics of the MIS structure are determined by various factors, but the properties of the dielectric and the dielectric-semiconductor interface play a special role [1–3]. Until recently, silicon dioxide (SiO_2) films were used as a dielectric in such structures, since its physical characteristics almost completely satisfy technological and operational requirements. Among inorganic solid materials, SiO_2 has the largest band gap (about 9 eV), is characterized by the highest resistivity (about 10^{23} Ohm·cm), and the glassiness and amorphousness of the films obtained by thermal oxidation in dry oxygen ensures their isotropy. However, the transition to nanotransistor electronics is faced with the problems of an ultra-thin dielectric [3], which is associated with the low dielectric constant of SiO_2 (3,8 – 3,9 a.u.). A decrease in the thickness of the SiO_2 film leads to the appearance of a tunneling current, decreases the breakdown voltage of the dielectric, and increases the effect of high-temperature technological modes on the properties of the dielectric-semiconductor interface.

This problem can be solved by replacing SiO_2 with a dielectric that has a higher dielectric constant and would meet the following conditions:

1. The technology for producing dielectric films must be compatible with the classical technology for manufacturing silicon MIS devices.

2. The process temperature is lower than the oxidation temperature of silicon in dry oxygen.

3. The quality of the dielectric-silicon interface is not worse than the $Si - SiO_2$ interface.

Therefore, the search and study of a dielectric alternative to silicon dioxide is an urgent task.

1 Problem statement

The simplest approach to choosing a dielectric for MIS structures is based on the relationship between the dielectric constant of a dielectric and its band gap, which determines the height of the potential barrier at the insulator-semiconductor interface [3]. Based on this, a group of dielectrics with increased dielectric constant (high-k), suitable for silicon MIS structures, is distinguished. High-k dielectrics include transition metal oxides and rare-earth metal oxides. These materials meet the technological requirements, and their relative permittivity lies in the range $\varepsilon = 8 \dots 30$. In this regard, there is an intensive study of candidates for replacing silicon dioxide, such as ZrO_2 [4,5], Al_2O_3 [1,6,7], Y_2O_3 [8], Gd_2O_3 [9,10], HfO_2 [11], CeO_2 [12] and others.

The increased dielectric constant of the dielectric makes it possible to increase the thickness of the dielectric film, which automatically excludes tunneling currents through it and increases the breakdown voltage. However, in addition to the dielectric constant, the parameters and characteristics of MIS devices are also influenced by other dielectric parameters: the degree of ionicity, the crystal lattice parameter, the effective charge in the dielectric and charge at the dielectric-semiconductor interface, work function and band gap [3].

Engström et al. [13] proposed a choosing criterion for a dielectric based on numerical simulation of the carrier tunneling process through a dielectric. This criterion only allows to reduce the range of suitable materials; numerical calculations are complex and their result is unique for each specific case of the dielectric thickness. Thus, after changing initial conditions, the simulation result may also change, therefore, a material change will be necessary in the technological process.

In works [3,14], choosing criteria, that are focused on the choice of a certain dielectric, was proposed. In accordance with these criteria, the most suitable is a dielectric with a largest value of a figure of merit, which depends on the set of dielectric parameters. Although this criterion assumes the choice of a certain dielectric, the choice result does not guarantee reliability, due to the optimal (reference) values are parameters of a hypothetical dielectric.

In addition, the considered criteria do not take into account the quality of the dielectric-semiconductor interface and are designed exclusively for a silicon substrate. However, the properties of the dielectric-semiconductor interface have an exceptional impact on the parameters and characteristics of MIS devices. In this regard, the problem arises of developing such a criterion for choosing a dielectric that would take into account the state of this interface for any semiconductor substrate.

In [2] general choosing criterion for a dielectric for any semiconductor substrate of an MIS structure theoretically obtained. This criterion is based on minimizing the value of the effective charge density at the dielectric-semiconductor interface. According to this criterion, the most satisfying the formulated requirements is cerium dioxide (CeO_2). Although this dielectric has already found practical application in MIS structures for various purposes, the properties of the CeO_2 – Si interface have not been sufficiently studied.

The purpose of this paper is experimentally confirm the choice of a dielectric based on this criterion. For this, it is necessary to determine the flat-band voltage and flat-band capacitance of MIS structures and quality assessment of the CeO_2 – Si interface.

The study was carried out by the capacitance-voltage (C-V) characteristics method. For the study, MIS structures were fabricated by oxidation of a metal mirror (substrate temperature was 160°C, chamber pressure was 10^{-5} Pa), on a silicon n-type substrate with volume resistivity 10 Ohm·cm. The thickness of the dielectric films was ~300 nm, the gate area A_G (the area of the metal electrode) was 1 mm^2.

2 Gate dielectric capacity

To determine the flat-band voltage and the charge density at the dielectric-semiconductor interface, it is necessary to know the gate dielectric capacitance of the MIS structure C_I [15]. This capacitance is part of the total structure capacitance C_{MIS}, which includes the capacitance C_I connected in series with parallel connection of the capacitance of the near-surface layer of the semiconductor C_{sc} and the charge capacity at the dielectric-semiconductor interface C_{it} (Fig. 1) [3].

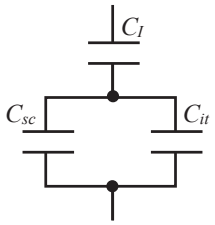

Fig. 1. Capacitive equivalent circuit of the MIS structure. C_I – dielectric capacitance, C_{sc} – capacitance of the near-surface layer of the semiconductor, C_{it} – charge capacity at the dielectric-semiconductor interface

In the case of a dielectric with a low dielectric constant, the gate capacitance is directly determined from the C-V characteristics of the MIS structure. It is equal to the capacitance in the saturation section of the C-V characteristic in the mode of enrichment of the near-surface layer of a semiconductor substrate with charge carriers. In this section of the C-V characteristic C_s is much larger than C_I and it can be assumed that the total capacity of the structure is determined only by the gate capacitance and does not depend on the gate voltage V_G.

A specific feature of the C-V characteristics of the $Al-CeO_2-Si$ structures (Fig. 2), in contrast to the C-V characteristics of the $Al-SiO_2-Si$ structure, it does not have a saturation region. This is due to the fact that the dielectric constant of CeO_2 is much higher comparing to SiO_2, and the capacitance C_I is quite large. In the enrichment mode, C_I is commensurate with the capacity C_{sc} and therefore the gate capacity cannot be separated from the total capacity of the structure C_{MIS}.

It should also be noted that, with a change in temperature, such MIS structures do not have a shift of the C-V characteristics along the stress axis (Fig. 2), which indicates the stability of the charge at the CeO_2-Si interface.

To determine the gate capacitance of the $Al-CeO_2-Si$ structures, the method described in [16] was used. The essence of this method is to plot the dependence $|dC_{MIS}/dV_G|^{1/2} = f(C_{MIS})$ using experimental C-V characteristics. In these coordinates, in the enrichment section of the C-V characteristic, it is a straight line. The point of intersection of this line with the abscissa gives the value of the gate capacitance.

Based on the real C-V characteristics data of the $Al-CeO_2-Si$ structure, a plot of the dependence is plotted $|dC_{MIS}/dV_G|^{1/2} = f(C_{MIS})$ (Fig. 3). From which it follows that the capacitance of the structure of a particular sample is 435 pF.

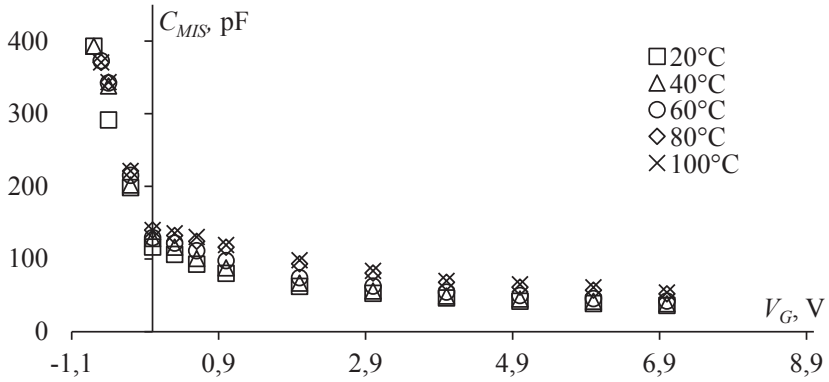

Fig. 2. High-frequency C-V characteristics of $Al-CeO_2-Si$ structures for different temperatures

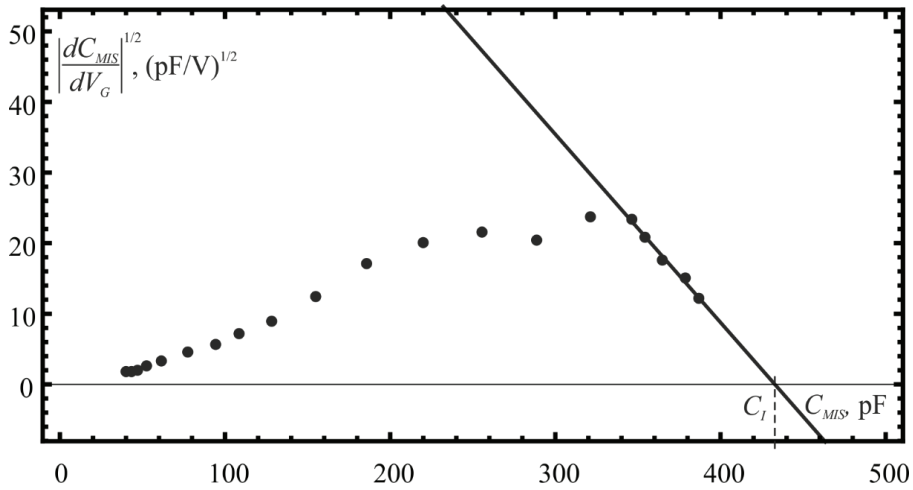

Fig. 3. Dependence $|dC_{MIS}/dV_G|^{1/2} = f(C_{MIS})$ for determining the gate capacitance C_I of the $Al-CeO_2-Si$ structure

3 The voltage and capacity of flat bands

The gate capacitance C_I does not depend on the voltage, so in determining the flat band voltage we will consider only a specific semiconductor and interface capacities:

$$c_s = c_{sc} + c_{it} = \left(\frac{1}{C_{MIS}/A_G} - \frac{1}{C_I/A_G}\right)^{-1}. \qquad (1)$$

Specific capacitance of the space charge region c_{sc} a depletion mode and weak inversion has the following

dependence of the surface potential ψ_s:

$$c_{sc} = \sqrt{\frac{\varepsilon_s \varepsilon_0 q N_{sub}}{\psi_s - \varphi_T}}, \quad (2)$$

and surface potential ψ_s is linearly related to gate voltage V_G:

$$V_G = V_{FB} + \frac{c_I - c_{it} - c^*_{sc}}{c_I}\psi_s, \quad (3)$$

where N_{sub} is impurity concentration in a semiconductor substrate; q is elementary electric charge; ε_0 is vacuum permittivity; ε_S is relative dielectric constant of a semiconductor; φ_T is temperature potential; V_{FB} is flat-band voltage; c_I is gate specific capacity; c^*_{sc} is specific capacity of the SCR, provided that $\psi_s = \varphi_0$; c_{it} is surface charge specific capacity. For simplicity, let us denote the constant factor in front of ψ_s by the coefficient n:

$$n = \frac{c_I - c_{it} - c^*_{sc}}{c_I}. \quad (4)$$

Substituting the surface potential ψ_s from (3) to (2) we obtain the dependence of the SCR capacity on the gate voltage:

$$c_{sc} = \sqrt{\frac{\varepsilon_s \varepsilon_0 q N_{sub}}{(V_G - V_{FB})\, n^{-1} - \varphi_T}}. \quad (5)$$

In the coordinates $c_{sc}^{-2}(V_G)$ this dependence is linear, and the point of its intersection with the voltage axis makes it possible to determine the flat-band voltage V_{FB}:

$$V_{FB} \approx V_G|_{C_{sc}^{-2}\to 0} - n \cdot \varphi_T. \quad (6)$$

By the tangent of the slope of this line k_{sc} coefficient n can be determined:

$$n = (k_{sc} \varepsilon_s \varepsilon_0 q N_{sub})^{-1}. \quad (7)$$

Based on the experimental data of the C-V characteristics of the structure (Fig. 2) the dependence $c_s^{-2}(V_G)$ for determining the flat-band voltage was plotted (Fig. 4). The plotted linear section of the dependence $c_s^{-2}(V_G)$, (which corresponds to the area of enrichment and weak inversion) by the method of least squares gives the value of the tangent $k_{sc} = 6 \cdot 10^{15}\mathrm{F}^{-2}\cdot\mathrm{cm}^4\cdot\mathrm{V}^{-1}$.

The concentration of the acceptor impurity $N_{sub} = N_A$ in the semiconductor substrate, determined from the Irwin curves [17], is $1{,}35\cdot10^{15}\mathrm{cm}^{-3}$.

Substituting value of k_{sc} and N_A in (7) we find that the coefficient n is 0,74.

Thus, according to the graph (Fig. 4) flat-band voltage of the test sample is $\sim 0{,}7$ V, and the capacitance corresponding to this voltage is 330 pF. Similar results were obtained for all structures of the batch in the amount of 10 samples (Table 1).

4 Charge density at the interface CeO_2 – Si

Surface charge density D_{it} and specific capacity c_{it} related by the ratio $c_{it} = q \cdot D_{it}$. Then from (4) we find:

$$D_{it} = \frac{c_I\,(1-n) - c^*_{sc}}{q}. \quad (8)$$

To determine the density of the surface charge, it is necessary to know c^*_{sc}, the value of which is found from (2) under the condition that $\psi_s = \varphi_0 = \varphi_T \cdot ln(N_{sub}/n_i)$. So, φ_0 = 0,296 V, and c^*_{sc} = $2{,}89\cdot10^{-8}$ F/cm. Substituting the data in (8) we obtain that the energy density of the charge at the CeO_2–Si interface is on average $2{,}5\cdot10^{11}\,\mathrm{eV}^{-1}\,\mathrm{cm}^{-2}$. This value corresponds to the charge density at the SiO_2–Si interface ($\sim 10^{11}\,\mathrm{eV}^{-1}\,\mathrm{cm}^{-2}$) of traditional MIS structures with SiO_2, films fabricated by thermal oxidation in dry oxygen.

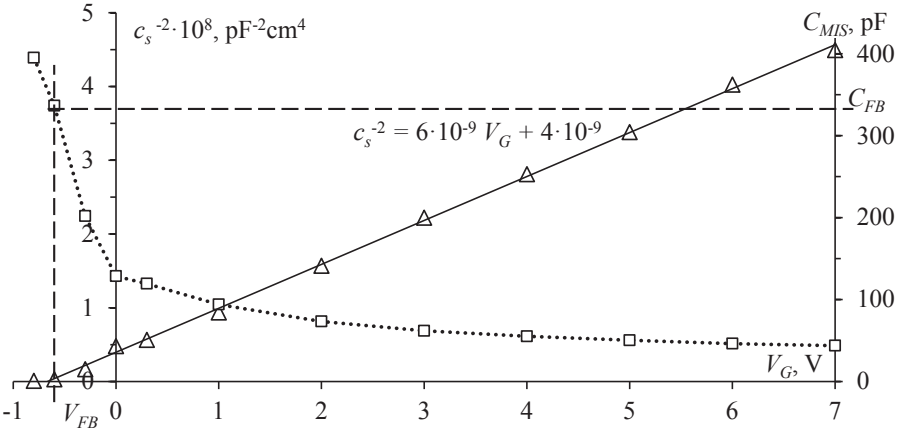

Fig. 4. Plot for determining the flat-band voltage V_{FB} and capacitance C_{FB} Al–CeO_2–Si structures. △ – $c_s^{-2}(V_G)$; □ – experimental C-V characteristic $C_{MIS}(V_G)$; – – – – flat-band voltage and capacitance

Табл. 1 Parameters of studied structures

Sample №	Flat-band voltage V_{FB}, V	Flat-band capacitance C_{FB}, pF	Energy density of the charge at the dielectric-semiconductor interface $D_{it}, eV^{-1}\text{cm}^{-2}$
1	0,7	330	$2{,}5 \cdot 10^{11}$
2	0,5	332	$2{,}5 \cdot 10^{11}$
3	0,3	325	$3{,}2 \cdot 10^{11}$
4	0,7	320	$1{,}4 \cdot 10^{11}$
5	0,8	334	$2{,}7 \cdot 10^{11}$
6	0,7	326	$2{,}4 \cdot 10^{11}$
7	0,9	333	$2{,}5 \cdot 10^{11}$
8	0,9	335	$2{,}6 \cdot 10^{11}$
9	0,7	315	$2{,}5 \cdot 10^{11}$
10	0,7	345	$2{,}3 \cdot 10^{11}$

Conclusions

1. The flat-band voltage and capacitance and the charge density of the CeO_2 – Si interface have been experimentally determined.

2. It is shown that the charge density at the CeO_2 – Si interface corresponds to the minimum values of the charge density at the SiO_2 – Si interface.

3. As the temperature changes, there is no shift in the C-V characteristic of the Al – CeO_2 – Si structures. This indicates the stability of the charge at the CeO_2–Si interface.

4. Significantly lower temperatures for obtaining CeO_2 films (160°C) in comparison with thermal oxidation of silicon in dry oxygen (> 1000°C), excludes the effect of high-temperature operations on their properties.

5. The obtained results indicate that CeO_2 films can be an alternative to SiO_2 films.Their use in MIS devices will eliminate the influence of tunneling currents, while maintaining the high quality of the dielectric-semiconductor interface.

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Експериментальне дослідження межі розділу діоксид церію – кремній МДН структур

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Робота присвячена актуальній задачі дослідження діелектрика альтернативного діоксиду кремнію в структурах метал-діелектрик-напівпровідник (МДН). У структурах метал-діоксид кремнію-кремній, при переході до нанорозмірів, товщина діелектричної плівки зменшується настільки, що стає тунельно-прозорою і знижується її напруга пробою. Виключити ці явища можна заміною діоксиду кремнію діелектриком з більш високою діелектричною проникністю. До таких діелектриків в першу чергу відносяться оксиди перехідних і рідкоземельних металів. Параметри і характеристики МДН структури визначаються різними факторами, але особливу роль відіграють властивості діелектрика і межі діелектрик-напівпровідник. У попередніх роботах авторів теоретично доведено, що діоксид церію з ряду діелектриків-претендентів повинен мати найкращу якість межі розділу з кремнієм. Дана робота присвячена дослідженню спрямованому на визначення напруги і ємності плоских зон МДН структур та на оцінку якості межі розділу діоксид церію – кремній. Дослідження проводиться методом вольт-фарадних характеристик. Для цього були виміряні високочастотні вольт-фарадні характеристики структур алюміній – діоксид церію – кремній за різних температур. Розглянуто ємність області просторового заряду (ОПЗ) в режимі збагачення і слабкої інверсії приповерхневого шару напівпровідника. Показано, залежність цієї ємності в (–2) ступеня від напруги на металевому електроді $c_s^{-2}(V_G)$ має лінійний характер. Перетин цієї лінії з віссю абсцис дає можливість визначити напругу плоских зон, а тангенс кута її нахилу – енергетичну щільність заряду на межі поділу діелектрик-напівпровідник. Показано, що щільність заряду на межі діоксид церію – кремній відповідає мінімальним значенням щільності заряду на межі діоксид кремнію – кремній. Відсутність зсуву вольт-фарадних характеристик досліджуваних структур при зміні температури свідчить про стабільність заряду на кордоні діоксид церію – кремній.

Ключові слова: МДН структура; діоксид церію; вольт-фарадна характеристика (ВФХ); напруга плоских зон; щільність заряду на межі поділу діелектрик-напівпровідник

Экспериментальное исследование границы раздела диоксид церия – кремний МДП структур

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Работа посвящена актуальной задаче исследования диэлектрика альтернативного диоксиду кремния в структурах метал-диэлектрик-полупроводник (МДП). В структурах метал-диоксид кремния-кремний, при переходе к наноразмерам, толщина диэлектрической пленки уменьшается настолько, что становится туннельно-прозрачной и снижается ее напряжение пробоя. Исключить эти явления можно заменой диоксида кремния диэлектриком с более высокой диэлектрической проницаемостью. К таким диэлектрикам в первую очередь относятся окислы переходных и редкоземельных металлов. Параметры и характеристики МДП структуры определяются различными факторами, но особую роль играют свойства диэлектрика и границы раздела диэлектрик-полупроводник. В предыдущих работах авторов теоретически доказано, что диоксид церия из ряда диэлектриков-претендентов должен иметь наилучшее качество границы раздела с кремнием. Эта работа посвящена исследованию направленному на определение напряжения и емкости плоских зон МДП структур и на оценку качества границы раздела диоксид церия – кремний. Исследование проводится методом вольт-фарадных характеристик (ВФХ). Для этого были измерены высокочастотные вольт-фарадные характеристики структур алюминий – диоксид церия – кремний при разных температурах. Рассмотрено емкость области пространственного заряда (ОПЗ) в режиме обогащения и слабой инверсии приповерхностного слоя полупроводника. Показано, что зависимость этой емкости в (–2) степени от напряжения на металлическом электроде $c_s^{-2}(V_G)$ имеет линейный характер. Пересечение этой линии с осью абсцисс дает возможность определить напряжение плоских зон, а тангенс угла ее наклона – энергетическую плотность заряда на границе раздела диэлектрик-полупроводник. Показано, что плотность заряда на границе диоксид церия – кремний соответствует минимальным значениям плотности заряда на границе диоксид кремния – кремний. Отсутствие сдвига ВФХ исследуемых структур при изменении температуры свидетельствует о стабильности заряда на границе диоксид церия – кремний.

Ключевые слова: МДП структура; диоксид церия; вольт-фарадная характеристика (ВФХ); напряжение плоских зон; плотность заряда на границе раздела диэлектрик-полупроводник