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Piezo Sensors Charge Amplifier for Quasi-Static and Single Measurements

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A charge amplifier is a key component of measurement systems based on piezoelectric transducers, as the accuracy of signal acquisition largely depends on its performance. While effective solutions exist for high-frequency applications, the implementation of charge amplifiers for quasi-static and single-shot measurements of signals containing a DC component remains challenging due to charge leakage from the storage capacitor, operational amplifier offset voltage drift, and sensitivity to common-mode interference. This paper proposes a novel charge amplifier architecture intended for quasi-static and single-shot measurements. The storage capacitor is placed outside the negative feedback loop, eliminating the need for a parallel discharge resistor and reducing charge losses during long measurement intervals. The scientific novelty of this study lies in the development of a charge amplifier architecture that separates the processes of piezoelectric sensor current amplification and charge storage, as well as in the proposed method for compensating offset-voltage-induced drift in the measurement circuit. In addition, the symmetrical input stage improves immunity to common-mode interference. A theoretical analysis of the major error sources, including capacitor self-discharge and operational amplifier offset effects, was carried out. Experimental validation of the proposed solution confirmed its suitability for quasi-static measurements and demonstrated improved performance compared with conventional charge amplifier topologies. The shortcomings of the prototype amplifier are also analyzed. Ways to overcome these shortcomings are proposed, and the prospects for the development of piezoelectric transducer charge amplifiers built on this principle are noted. In particular, implementing the amplifier as part of a specialized integrated circuit for piezoelectric measuring systems will significantly improve its characteristics.

Keywords: charge amplifier; piezoelectric transducer; quasi-static measurement; low-frequency signal conditioning; offset voltage compensation; common-mode noise rejection; measurement electronics

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Introduction

Voltage amplifiers and charge amplifiers are used to amplify piezoelectric sensor signals. Charge amplifiers are often preferred because the topology of charge amplifiers makes them insensitive to the capacitance of the connecting cables [1]. Voltage amplifiers, on the other hand, are very sensitive to the capacitance of the connecting cable and require recalibration when replacing it. This article will focus on charge amplifiers.

A simplified schematic diagram of a typical charge amplifier is shown in Fig. 1. As can be seen from Fig. 1, the piezoelectric sensor is connected between ground and the “virtual ground”, because of which the voltage across the sensor is always zero. This fact is the reason for the insensitivity of the charge amplifier to the capacitance of the connecting cable.

The amplifier functions as follows: capacitor C is charged to voltage U_{out} by transducer current I_s .

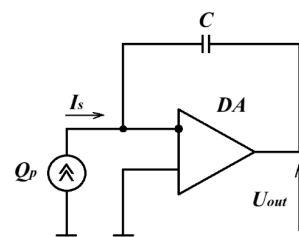


Fig. 1. Simplified schematic diagram of a charge amplifier

The current in the transducer is generated when it is deformed as a result of the direct piezoelectric effect, i.e.

$$U_{out} = \frac{Q_s}{C},$$

where U_{out} is the output voltage of the charge amplifier, $Q_s = \int_0^T i_s dt$ is the charge generated at the electrodes of the piezoelectric transducer Q_p , and C is the feedback capacitance. Or

$$\frac{U_{out}}{Q_s} = \frac{1}{C}. \quad (1)$$

As is well known, the charge Q_s is proportional to the pressure on the transducer electrodes; consequently, the output voltage of the charge amplifier is also proportional to the pressure on the transducer electrodes. By knowing the area of the transducer electrodes, it is possible to determine the force causing this pressure.

The simplified diagram in Fig. 1 is an idealized representation. For the amplifier to operate correctly, it is necessary to ensure that a bias current flows through the inverting input. This is achieved by modifying the circuit, as shown in Fig. 2.

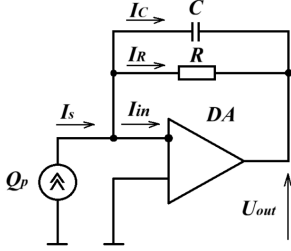


Fig. 2. Complete circuit diagram of the charge amplifier
For this circuit, the following system of equations can be written:

$$\begin{cases} U_{out} = \frac{1}{C} \int I_c dt, \\ I_c = I_s - I_R - I_{in}, \\ I_R = \frac{U_{out}}{R}, \\ I_{in} = \frac{U_{out}}{R_{in}}, \end{cases}$$

where I_c is the capacitor charging current, I_R is the current through resistor R , I_{in} is the input current of the inverting input, R is the circuit resistance, and R_{in} is the input resistance of the inverting input.

Or, by applying the Laplace transform:

$$\begin{cases} U_{out}(p) = \frac{I_c(p)}{pC}, \\ I_c(p) = I_s(p) - I_R(p) - I_{in}(p), \\ I_R(p) = \frac{U_{out}(p)}{R}, \\ I_{in}(p) = \frac{U_{out}(p)}{R_{in}}, \end{cases}$$

where p is the Laplace complex frequency variable. From this system of equations, consider that

$$\frac{I_s(p)}{p} = Q_s(p)$$

we can obtain:

$$U_{out}(p) = \frac{Q_s(p)}{C} \frac{pR_{\Sigma}C}{1 + pR_{\Sigma}C}, \quad (2)$$

where $R_{\Sigma} = \frac{R \cdot R_{in}}{R + R_{in}}$.

If $R_{in} \gg R$, then the effect of the input resistance R_{in} can be neglected, and formula (2) can then be written as:

$$U_{out}(p) = \frac{Q_s(p)}{C} \frac{pRC}{1 + pRC}.$$

Therefore, resistor R allows the input current to flow through the operational amplifier, but this circuit is unsuitable for quasi-static operation. By ‘quasi-static mode’ we mean an operating mode in which the charging rate of the capacitor C is low, and the charge Q_s applied to this capacitor is retained for a long time.

The cut-off frequencies of the transducer signals, above which the effect of resistor R on the amplifier’s output voltage (and the measurement accuracy) can be considered negligible, can be defined as:

$$\omega_s > \frac{10}{RC},$$

where ω_s is the angular frequency of the input signal (an error of approximately 1 – 0.5%).

For typical values of $R = 10$ Mohm and $C = 1$ nF, the cut-off frequency is $\omega_s = 1000$ rad/s, or $f_s = 160$ Hz.

Consequently, the task of broadening the bandwidth of charge amplifiers in the low-frequency range remains a pressing issue, and numerous articles [2–15] have been devoted to this topic. Article [2] proposes a charge amplifier which, thanks to a slight complication of the circuit compared to the classic design shown in Fig. 2, provides a lower cut-off frequency of $f_s = 0,2$ Hz, as well as a low bias voltage of $U_{off} \approx 210 \mu V$. However, the amplifier proposed in [2] does not provide offset voltage compensation for a unipolar output voltage. It also does not support single-measurement mode for unipolar signals.

1 Charge amplifier for quasi-static measurement mode

This article proposes a charge amplifier topology that enables quasi-static operation (i.e. single charge measurements) and is characterized by significantly lower sensitivity to in-phase noise. A simplified diagram of the amplifier is shown in Fig. 3. In this amplifier, the process of ‘transferring’ charge from the piezoelectric sensor to the capacitor is divided into two stages. First, the sensor current is amplified, and then the capacitor is charged with a current proportional to the sensor current. Preliminary amplification of the sensor current will allow for an increase in the capacitance in which the charge is stored. An increased capacitance of the capacitor will be less sensitive to the discharge current caused by the presence of an external load. This will improve the accuracy of the measurements, as the capacitor will be discharged more slowly.

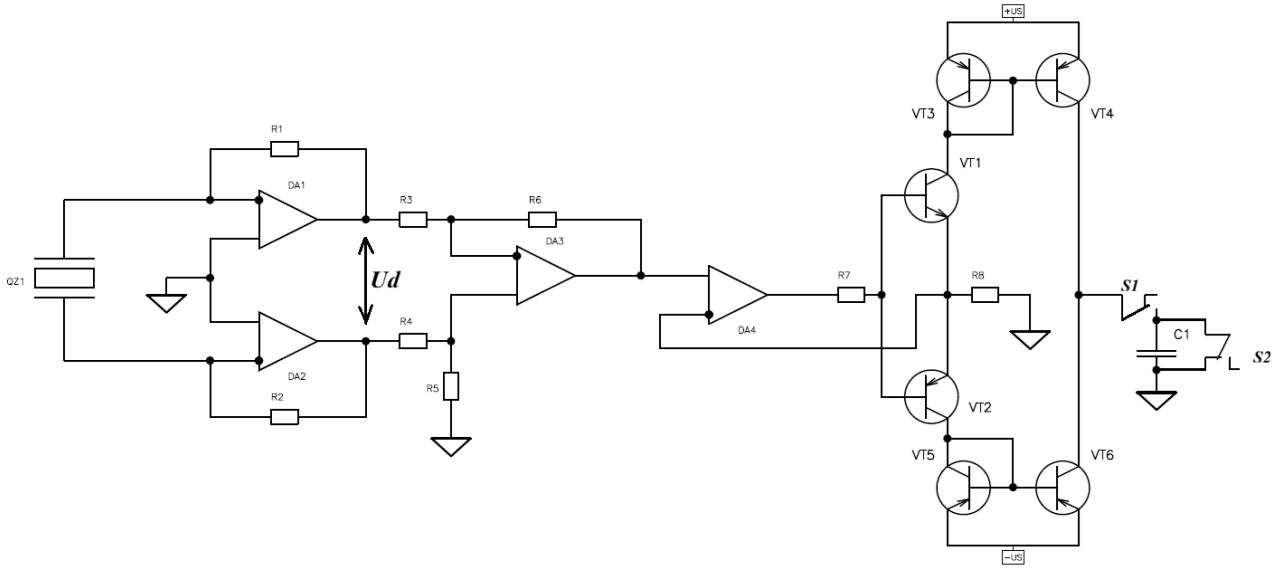


Fig. 3. Proposed circuit diagram of a charge amplifier suitable for quasi-static measurements

The amplifier shown in Fig. 3 operates as follows: the current from the piezoelectric sensor QZ1, flowing through the feedback resistors of the balanced inverting amplifier which consist of DA1 and DA2, causes an output voltage U_d to appear at the outputs of the operational amplifiers DA1 and DA2. This voltage is amplified by the differential amplifier DA3. The current amplifier, which consist of the voltage follower DA4 and the two current mirrors VT3–VT6, charges the measuring capacitor C1 with a current proportional to the output voltage of the differential amplifier DA3. Immediately before the measurements, switch S2 is opened. Before this, switch S2 keeps capacitor C1 discharged. At the same time, switch S1 is closed, connecting the measuring capacitor to the amplifier output. Switch S1 remains in the closed position until the measurements are complete. The criterion for terminating the measurements, particularly in the case of an aperiodic process, may be the attainment of a zero current level in sensor QZ1. An aperiodic process may occur when using an aperiodic excitation mode for the piezoelectric transducer [3, 4]. Once the measurements are complete, switch S1 opens, putting capacitor C1 into charge-holding mode. Once the measurement results have been processed, switch S2 closes, discharging capacitor C1. Thus, the measuring capacitor C1 and the amplifier are switched to standby mode in preparation for the next measurement.

Let $R1 = R2 = R_{iQz}$, $R4 = R3 = R'$, $R5 = R6 = R''$, and $R8 = R_{iC}$, in the circuit shown in Fig. 3. Then the expression for the output voltage is:

$$U_{C1} = \frac{Q_s}{C1} \cdot \frac{2 R_{iQz}}{R_{iC}} \cdot \frac{R''}{R'} , \quad (3)$$

where U_{C1} is the voltage across capacitor C1, R_{iQz} is the equivalent input resistance of the sensor branch, R_{iC} is the equivalent resistance of the capacitor-charging branch, and R' , R'' are the resistances of

the differential-stage branches. To achieve equivalence between the output voltage (3) of the proposed amplifier and the output voltage of the idealised amplifier (Fig. 1), the capacitance of the measuring capacitor C1 must be equal to:

$$C1 = C \cdot \frac{2 R_{iQz}}{R_{iC}} \cdot \frac{R''}{R'} .$$

Capacitors with a higher capacitance discharge more slowly under an external load and can provide a longer measurement time.

2 Analysis of the errors in the proposed charge amplifier

Errors that arise during measurements can be divided into two categories:

1. Errors arising during the charging of capacitor C1.
2. Errors arising during the storage of the charge in capacitor C1.

Errors in charge storage are caused by the self-discharge current I_{dch} of capacitor C1 and the discharge current I_{S2} through the resistance of the open switch S2. Thus, we can write:

$$U_{C1}(t) = U_{C1}(0) - \frac{1}{C1} \int_0^t (I_{dch}(t) + I_{S2}(t)) dt ,$$

where t is time, and τ is the integration interval (measurement duration). In differential form:

$$\frac{dU_{C1}(t)}{dt} = \frac{1}{C1} U_{C1}(t) \frac{R_{dch} + R_{S2}}{R_{dch} \cdot R_{S2}} - \frac{U_{C1}(t)}{C1 \cdot R_l} ,$$

where R_{S2} and R_{dch} are the open-circuit resistance of switch S2 and the leakage resistance of capacitor C1,

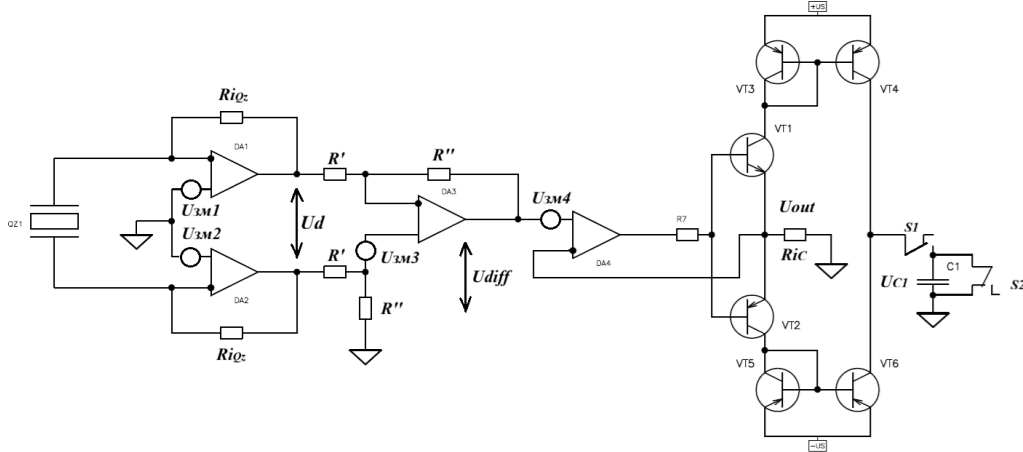


Fig. 4. Diagram for analyzing the effect of operational amplifier offset voltages on the accuracy of the output voltage

respectively, R_l is the equivalent leakage resistance, and these resistances are assumed to be independent of the applied voltage.

$$R_{\parallel} = \frac{R_{dch} + R_{S2}}{R_{dch} \cdot R_{S2}},$$

where $R_{\parallel}$ is the equivalent parallel resistance. The solution to this equation is the function:

$$U_{C1}(t) = U_{C1}(0)e^{-\frac{t}{C1 \cdot R_{\parallel}}}.$$

From this expression, it is possible to determine the maximum duration of the measurement processing, during which the measuring capacitor C1 will discharge to a level no lower than the specified value:

$$\tau = -R_{\parallel} |C1 \cdot \ln \alpha|, \quad (4)$$

where $\alpha = \frac{U_{C1}(\tau)}{U_{C1}(0)}$, $U_{C1}(\tau) = U_{C1}(0) \left(1 - \frac{\delta}{100}\right)$, and δ is the permissible capacitor discharge, in per cent, as specified by the measurement accuracy requirements.

A capacitor with an NP0 (*Negative-Positive-Zero temperature coefficient*) dielectric and a capacitance of $0.1 \mu\text{F}$ has a leakage resistance [16] $R_{dch} = 1 \times 10^{11} \text{ Ohm}$; the switch based on field-effect transistors within the CD4066 (*CMOS Quad Bilateral Switch*) integrated circuit has an on-resistance [17], $R_{S2} = 1 \times 10^{11} \text{ Ohm}$; therefore, $R_{\parallel} = 0.5 \cdot 10^{11}$. According to formula (4), the measuring capacitor will discharge by 1 % in $\tau = -0.5 \cdot 10^{11} \cdot 0.1 \cdot 10^{-6} \ln 0.99 \approx 5 \text{ s}$, which is more than sufficient for carrying out measurements.

The errors that arise during the charging of the capacitor are mainly due to the offset voltages of the operational amplifiers. A circuit for analysing the effect of offset voltages on the accuracy of the output voltage is shown in Fig. 4.

The output voltage U_d of a balanced inverting amplifier with amplifier bias voltages U_{off1} and U_{off2} is equal to:

$$U_d = 2 R_{iQz} \cdot I_s + |U_{off1}| + |U_{off2}|.$$

The output voltage of the differential amplifier U_{diff} with a bias voltage U_{off3} is equal to:

$$U_{diff} = [2 R_{iQz} \cdot I_s + |U_{off1}| + |U_{off2}|] \cdot \frac{R''}{R'} + |U_{off3}| \left[1 + \frac{R''}{R'}\right].$$

The voltage U_{out} is equal to:

$$U_{out} = [2 R_{iQz} \cdot I_s + |U_{off1}| + |U_{off2}|] \cdot \frac{R''}{R'} + |U_{off3}| \left[1 + \frac{R''}{R'}\right] + |U_{off4}|,$$

where U_{off4} is the bias voltage of the output stage. The output voltage of the amplifier (the voltage across capacitor C1) is equal to:

$$U_{C1} = \frac{1}{C1 \cdot R_{ic}} \left([2 R_{iQz} \cdot I_s + |U_{off1}| \cdot \tau + |U_{off2}| \cdot \tau] \cdot \frac{R''}{R'} + |U_{off3}| \left[1 + \frac{R''}{R'}\right] \cdot \tau + |U_{off4}| \cdot \tau \right), \quad (5)$$

where τ is the time when switch S1 is closed.

As can be seen from equation (5), the bias voltages of the operational amplifiers result in an additional error voltage, which, at the end of the measurement, is:

$$\Delta U_{C1} = \frac{1}{C1 \cdot R_{ic}} \left([U_{off1} \cdot \tau + U_{off2} \cdot \tau] \cdot \frac{R''}{R'} + |U_{off3}| \left[1 + \frac{R''}{R'}\right] \cdot \tau + U_{off4} \cdot \tau \right). \quad (6)$$

It can be seen from equation (6) that the offset voltages of amplifiers DA1–DA3 have the greatest influence on the magnitude of the error, as they are multiplied by the corresponding gain factor.

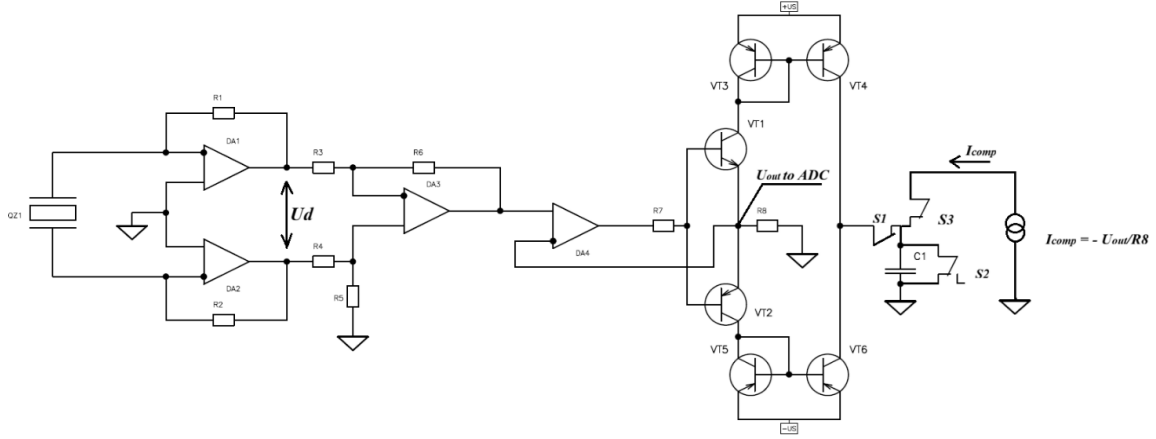


Fig. 5. Schematic diagram of a charge amplifier with compensation for the effect of bias voltages on the capacitor charge

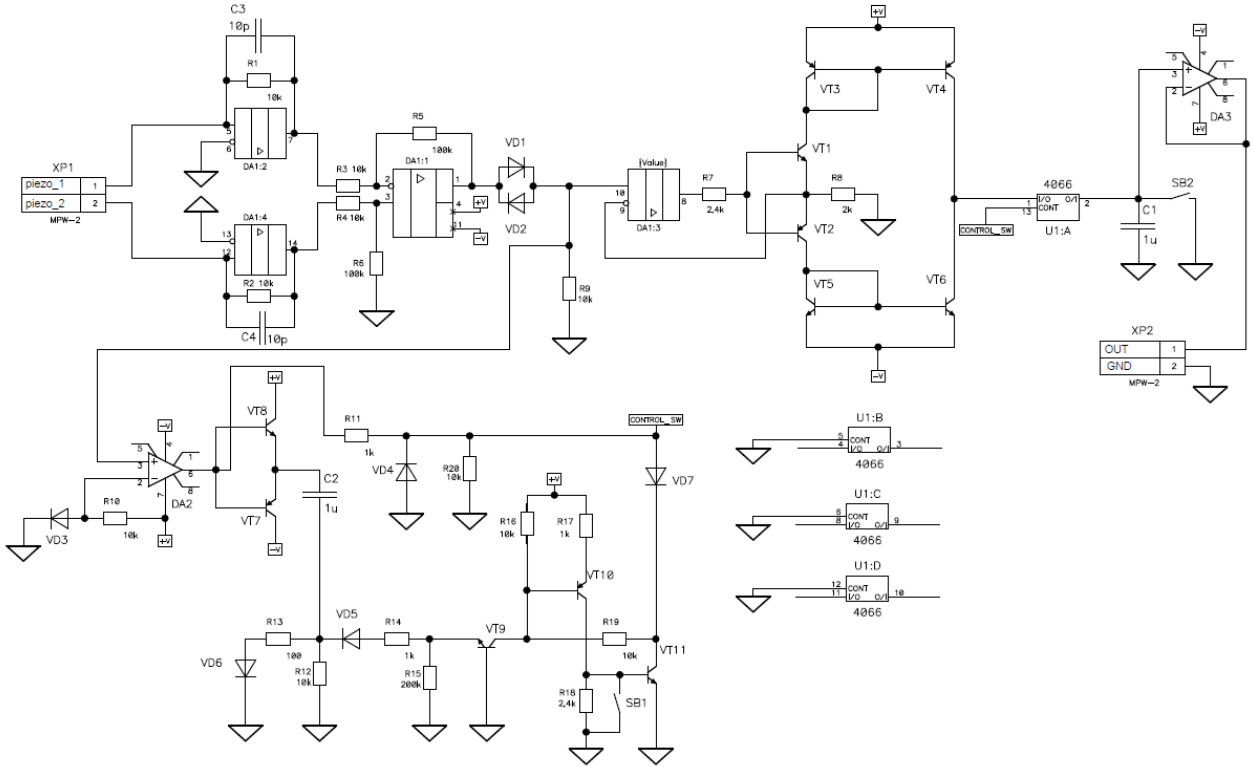


Fig. 6. Schematic diagram of a charge amplifier for quasi-static measurements

The most unfavorable situation arises when all the offset voltages have the same sign. It is also possible to partially compensate for the bias voltages of the amplifiers, particularly when the amplifiers are of the same type, i.e. they have the same probability density function for the bias voltages.

The problem of zero drift caused by offset voltage is discussed in [8]. To compensate for the effects of the charge amplifier's offset voltage, a digital automatic control system based on a PI (*Proportional-Integral*) controller and a master controller is proposed. This master controller calculates the parameters of the PI controller and sets the sampling rate of the data

board's ADC (*Analog-to-Digital Converter*). A charge amplifier with such a compensation system has a lower cut-off frequency of $f_s = 1 \text{ mHz}$, but cannot process signals containing a DC (*Direct Current*) component in single-shot measurement mode.

In the proposed amplifier, to compensate for the effect of the offset voltage ΔU_{C1} , the voltage U_{out} across resistor R_{ic} is measured immediately prior to the main measurements (Fig. 5). At the same time as the measurements begin, and in synchronization with the closing of switch S1, close switch S3 to start charging capacitor C1 with a current of $I_{comp} = -\frac{U_{out}}{R_{ic}}$. Thus, the drift in the output voltage caused by the charge on

the measuring capacitor C1 is fully compensated. The temperature drift of the bias voltages during quasi-static measurements (10–100 s) is small. The circuit diagram of the charge amplifier with the proposed zero-drift compensation system is shown in Fig. 5

A prototype was built to test the proposed amplifier; its circuit diagram is shown in Fig. 6 (without an offset voltage compensation system).

The charge amplifier itself consists of operational amplifiers DA1.1–DA1.4 and DA3, transistors VT1–VT6, field-effect transistor switches within the CD4066 integrated circuit, resistors R1–R9, diodes VD1 and VD2, and capacitor C1. The part of the circuit comprising the operational amplifier DA3, transistors VT7–VT11, capacitor C2, resistors R10–R19, diodes VD3–VD7, and switches SB1 and SB2 forms a comparator and a trigger. This part of the circuit connects capacitor C1 to the amplifier output via the CD4066 switch when a positive current is present and disconnects C1 when the current reaches zero. In this way single-measurement mode is implemented. Figure 7 shows the waveforms of the characteristic voltages that occur in the amplifier during measurements.

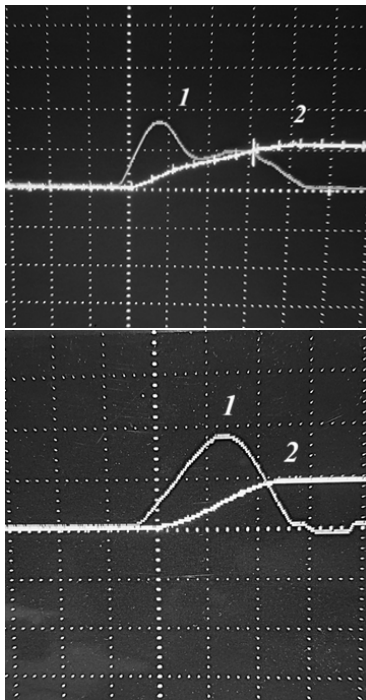


Fig. 7. Quasi-static measurements. Weighing a load of 0.25 g: 1 – voltage proportional to the piezoelectric transducer current; 2 – voltage across the capacitor

The scale division for curve 1 is 5 V per division, for curve 2 – 1 V per division. The time scale is 50 μ s per division.

The prototype circuit shown in Fig. 6 is not without its drawbacks. The most important of them is a certain disproportionality of the capacitor charging current to the input current of the current mirrors (current through resistor R8). This disproportionality is due to

the Early effect. To reduce the influence of the Early effect, it is advisable to use Wilson current sources.

Conclusions

For quasi-static and single-shot measurements, it is important to minimise the discharge current of the capacitor in which the piezoelectric transducer's charge is stored. In classical charge amplifier circuits, this capacitor forms part of the negative feedback loop. To ensure the amplifier functions correctly, a resistor must be connected in parallel with the capacitor, which significantly limits the performance of conventional charge amplifiers when performing quasi-static and single-shot measurements. This paper proposes an amplifier in which the capacitor is located outside the negative feedback loop and therefore does not require the connection of an additional parallel resistor. The amplifier also amplifies the piezoelectric transducer current, allowing the use of a capacitor with a higher capacitance, which discharges more slowly to the external load. Furthermore, due to the symmetry of the input circuit, the proposed amplifier is less sensitive to common-mode interference.

It is promising to implement the amplifier as a component of a specialized integrated circuit for piezoelectric measuring systems. An integrated amplifier, due to the identity of the components, will have significantly better characteristics. In the integrated version, it is possible to compensate for charge injection into the measuring capacitor when switching keys on CMOS structures, for example, by using dummy transistors. In addition, integrated amplifiers usually have better reliability.

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Підсилювач заряду для квазістатичних і одиничних вимірювань

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Підсилювач заряду є ключовим елементом вимірювальних систем на основі п'єзоелектричних перетворювачів, оскільки точність реєстрації сигналів значною мірою визначається його характеристиками. Для високочастотних сигналів існують ефективні технічні рішення, однак реалізація підсилювачів для квазістатичних та одиничних вимірювань сигналів із постійною складовою

залишається складною через розряд накопичувального конденсатора, вплив напруги зміщення операційних підсилювачів та високу чутливість до синфазних завад.

У роботі запропоновано нову архітектуру підсилювача заряду для квазістатичних і одиничних вимірювань, у якій накопичувальний конденсатор винесено за межі кола негативного зворотного зв'язку, що усуває необхідність використання паралельного резистора розряду та зменшує втрати заряду під час тривалих вимірювань. Наукова новизна полягає у розробці схеми підсилювача заряду з розділенням процесів підсилення струму п'єзодатчика та накопичення заряду, а також у запропонованому методі компенсації дрейфу, спричиненого напругою зміщення операційних підсилювачів. Завдяки симетричній структурі вхідного каскаду також досягнуто зниження чутливості до синфазних завад.

Проведено теоретичний аналіз основних джерел похибок, зокрема саморозряду накопичувального конденсатора та впливу напруг зміщення активних елементів. Експериментальна перевірка працездатності запропонованого рішення підтвердила можливість його використання для квазістатичних вимірювань із підвищеною точністю порівняно з класичними схемами підсилювачів заряду.

Проаналізовано недоліки прототипу підсилювача. Запропоновано шляхи подолання цих недоліків, вказано перспективи розвитку підсилювачів заряду п'єзоперетворювачів, побудованих за принципом розділення процесів підсилення струму п'єзодатчика та накопичення заряду. Зокрема, виконання підсилювача як частини спеціалізованої інтегральної мікросхеми для п'єзоелектричних вимірювальних систем дозволить значно покращити його характеристики.

Ключові слова: підсилювач заряду; п'єзоелектричний перетворювач; квазістатичні вимірювання; обробка низькочастотних сигналів; компенсація напруги зміщення; пригнічення синфазних завад; вимірювальна електроніка